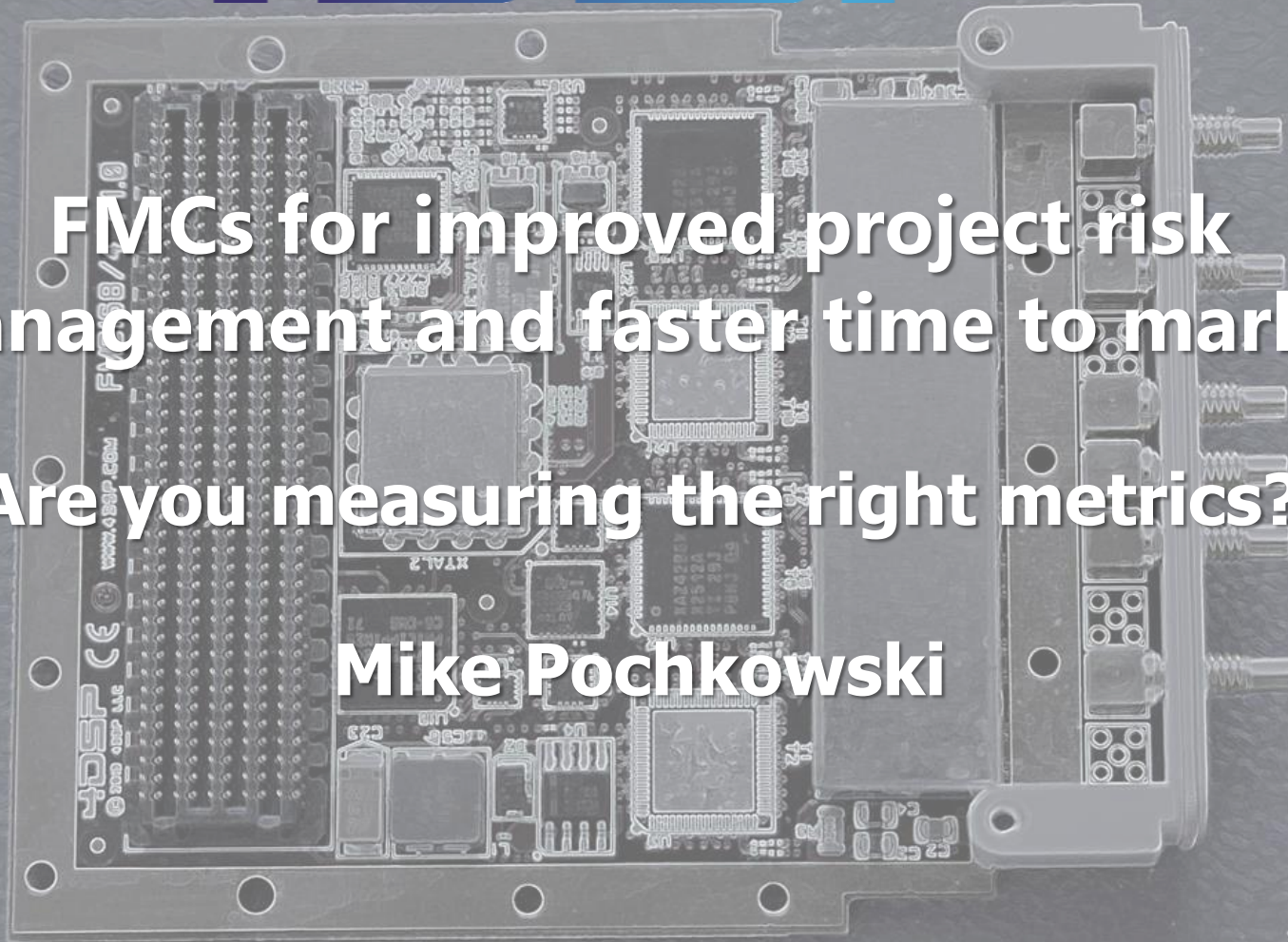


# **4D SP**

**FMCs for improved project risk management and faster time to market**

**Are you measuring the right metrics?**

**Mike Pochkowski**



# Outline

- FMC Overview
  - Features which motivate designers and integrators
- Metrics
  - Metrics that motivate program managers, execs, and corporate stakeholders
- Risk Minimization and Faster Time to Market Development Strategy
- FMC: A sure bet for a solution ready on time

# FMCs:

## Flexibility & Ease of System Development

- Today's FPGAs are really SoCs; Latest Gen offers

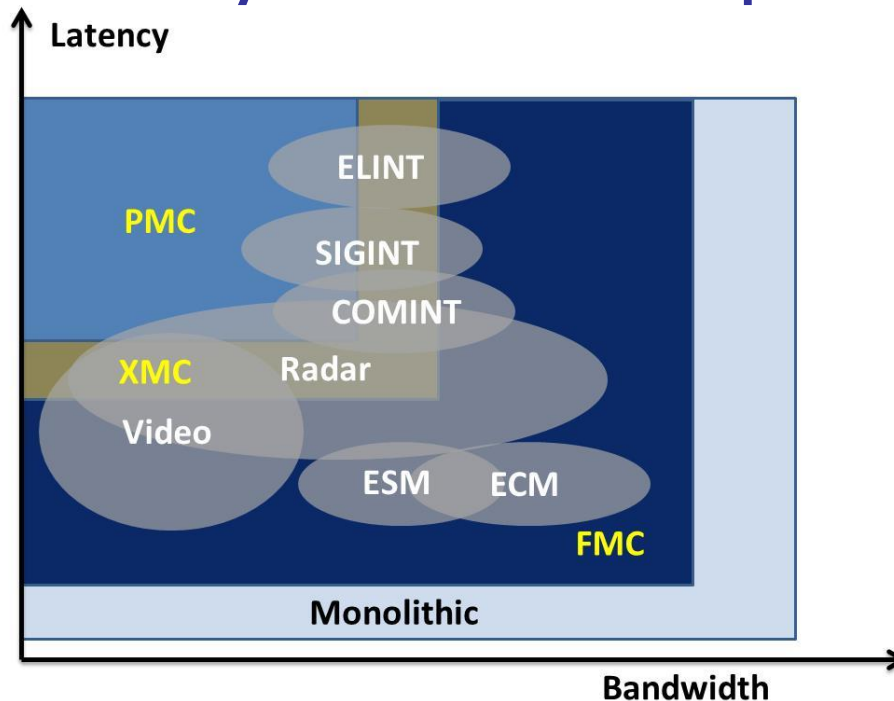
	<b>Current Technology FPGA</b>
Logic Cells	326K–693K
CLB	408K–864K
Block RAM (kb)	27,000–52,920
DSP Slices	1,120–3,600
Serial Gbit Transceivers	28–80
User I/O	700–1,000

- FPGA-FMC: The perfect combination for optimal performance and flexibility
  - Addresses the bandwidth, latency, and connectivity limitations of PMC and XMC
  - FMC 1/2 size of XMC; <10W of heat
  - Becoming easier to integrate FMC and FMC carrier cards from different vendors (VITA 57.2)

# FMCs:

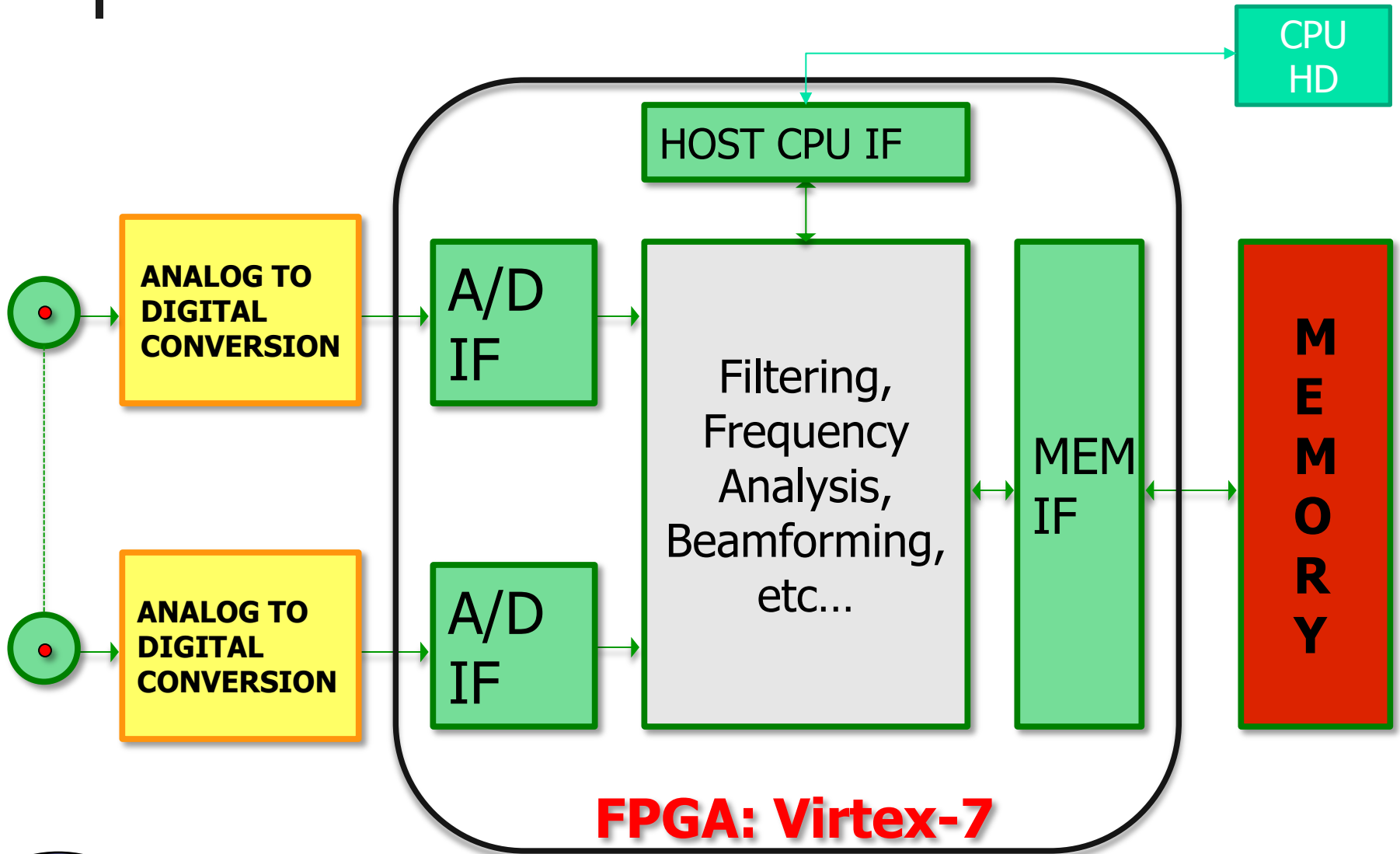
## Flexibility & Ease of System Development

- Applications
  - Intelligence Systems
  - Real-time Video Processing
  - Surveillance
  - Reconnaissance
  - Counter Measures



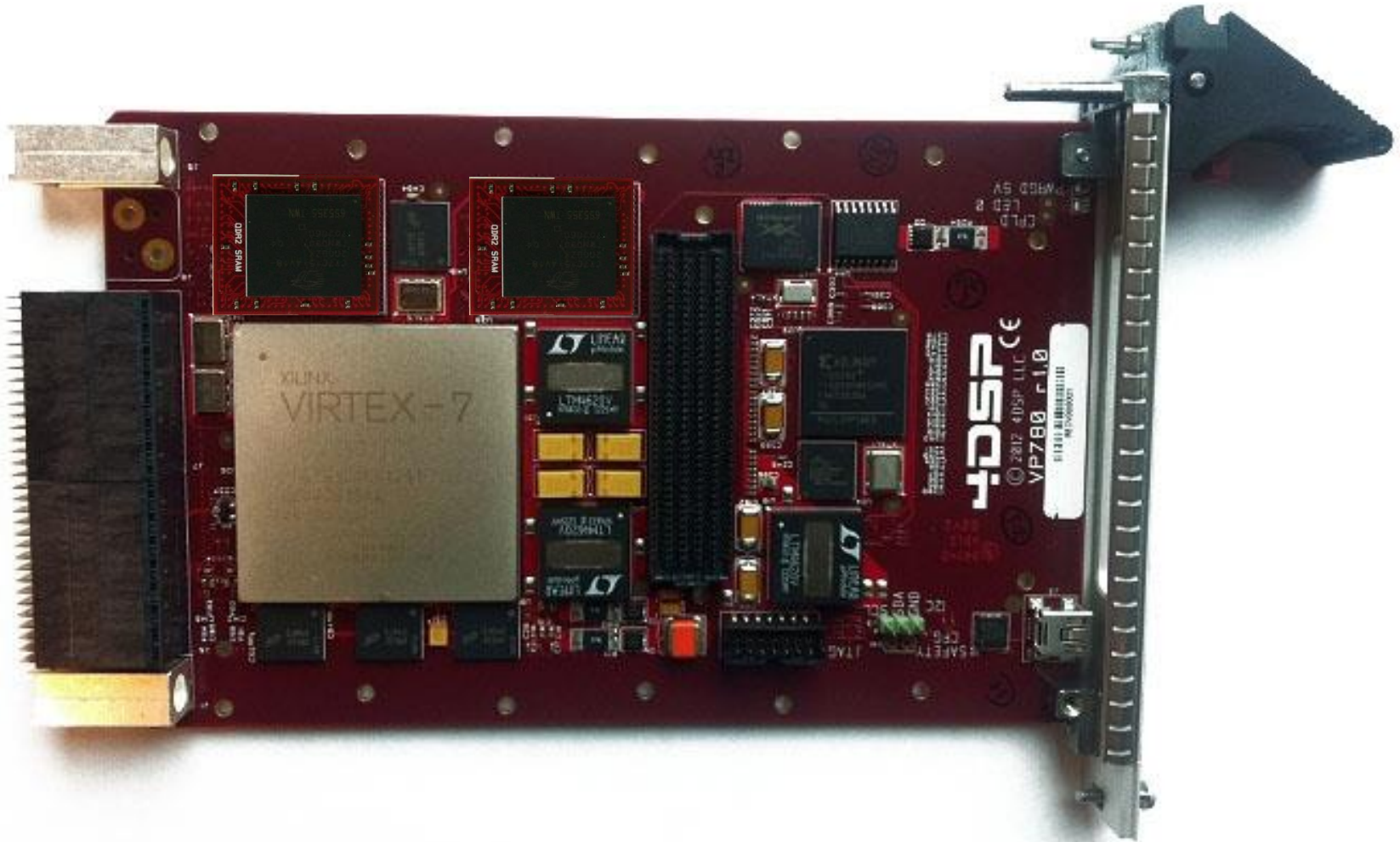
- Simply great for system upgrades and technology insertion
- Customization – Easier to track new technologies as they become available (higher resolution A/Ds and D/As)
- Flexibility to reuse carrier, firmware, and software on new projects
- Standardized engineering knowledge base while decreasing spin up time on new projects and programs

# Typical DAQ architecture

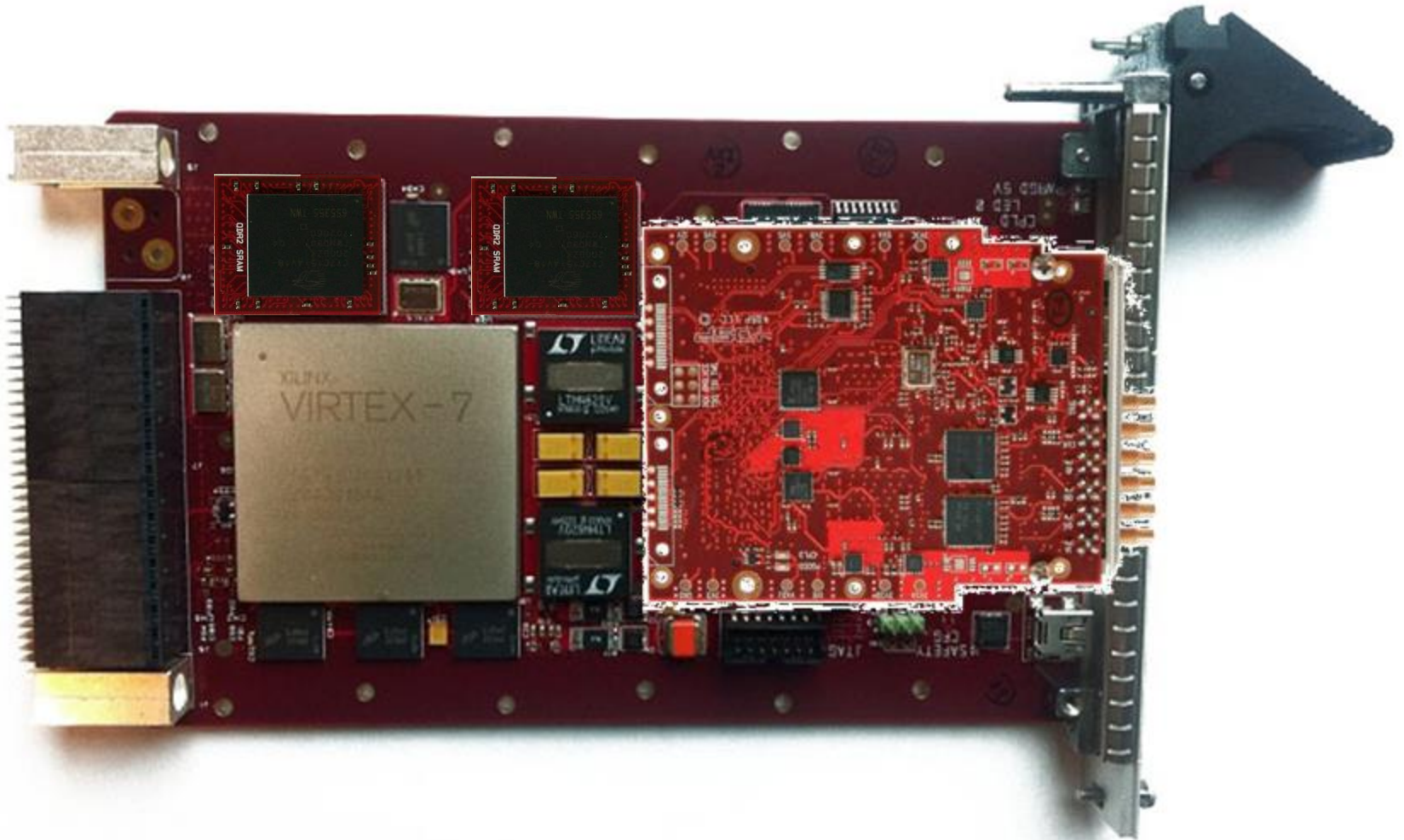




# Exploring a potential solution



# Exploring a potential solution

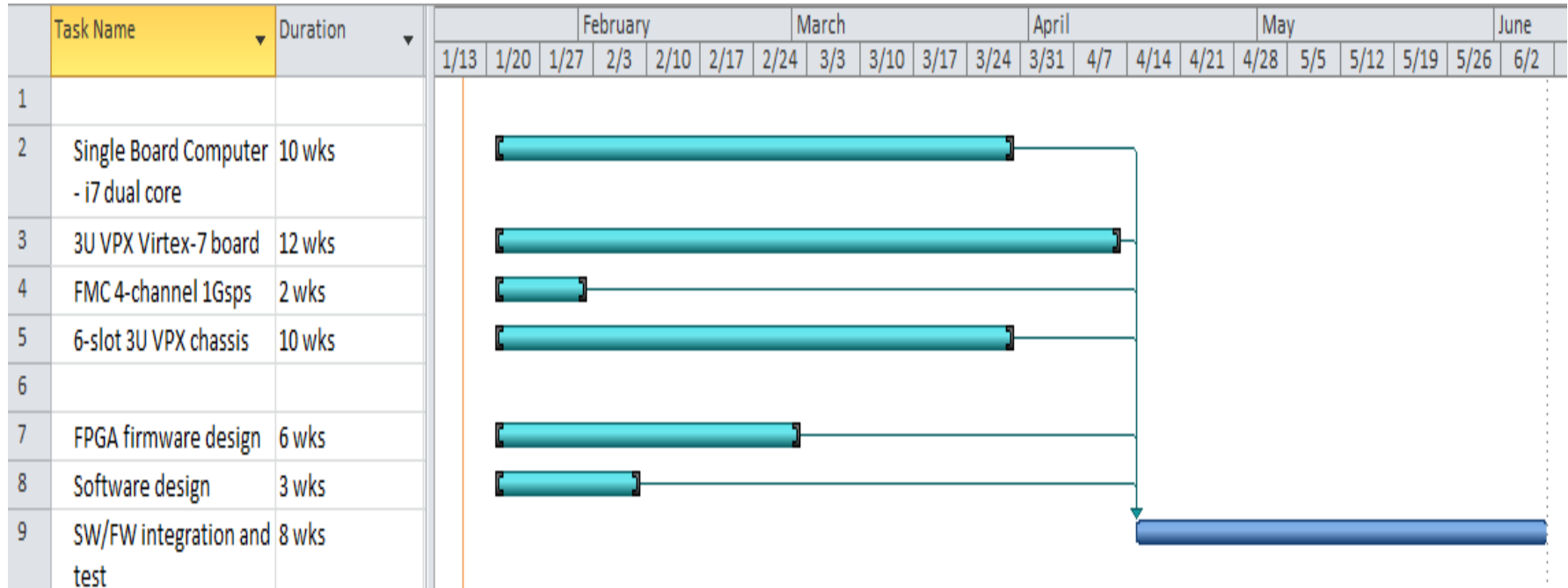


# Exploring a potential solution





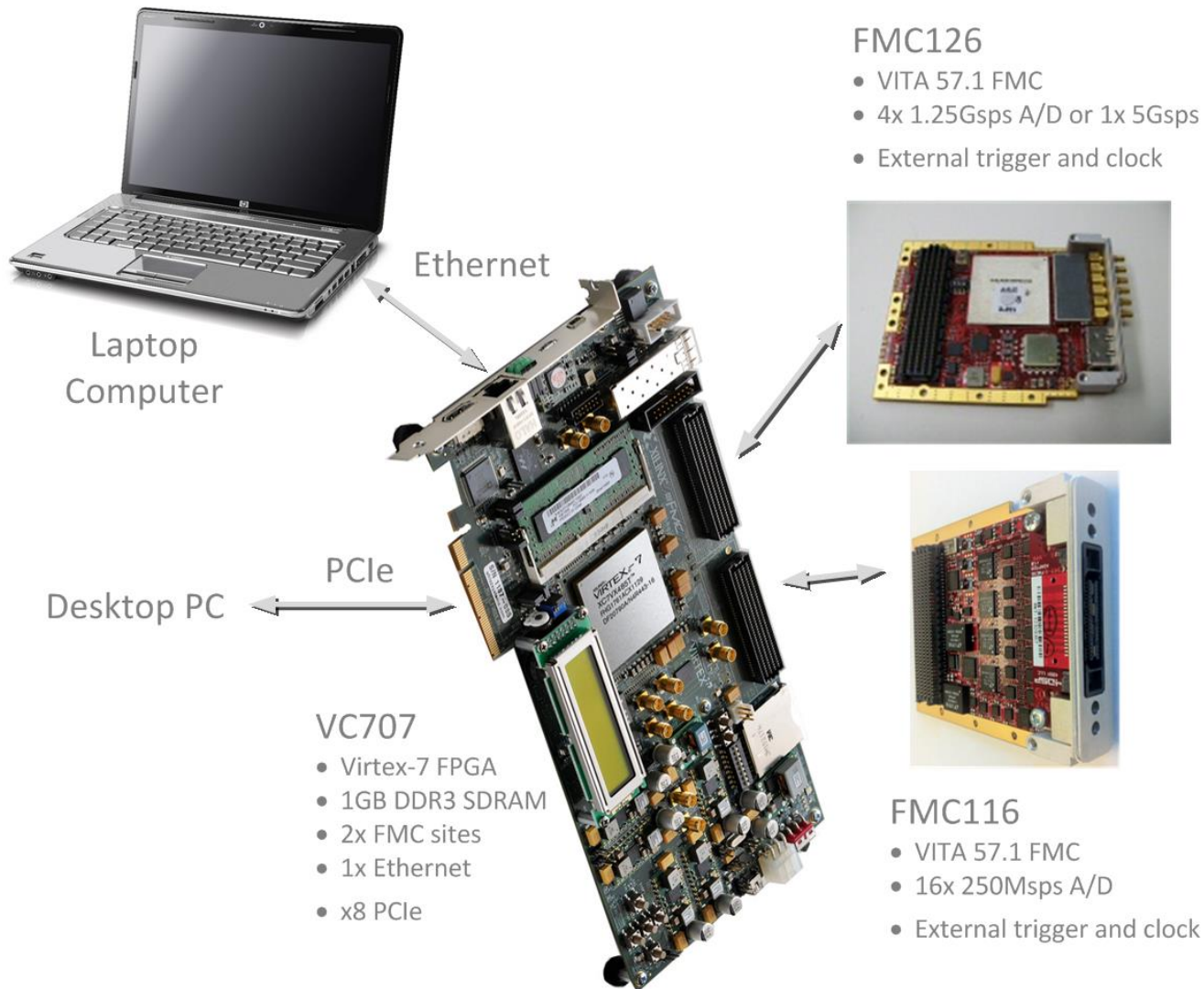
# Exploring a potential solution



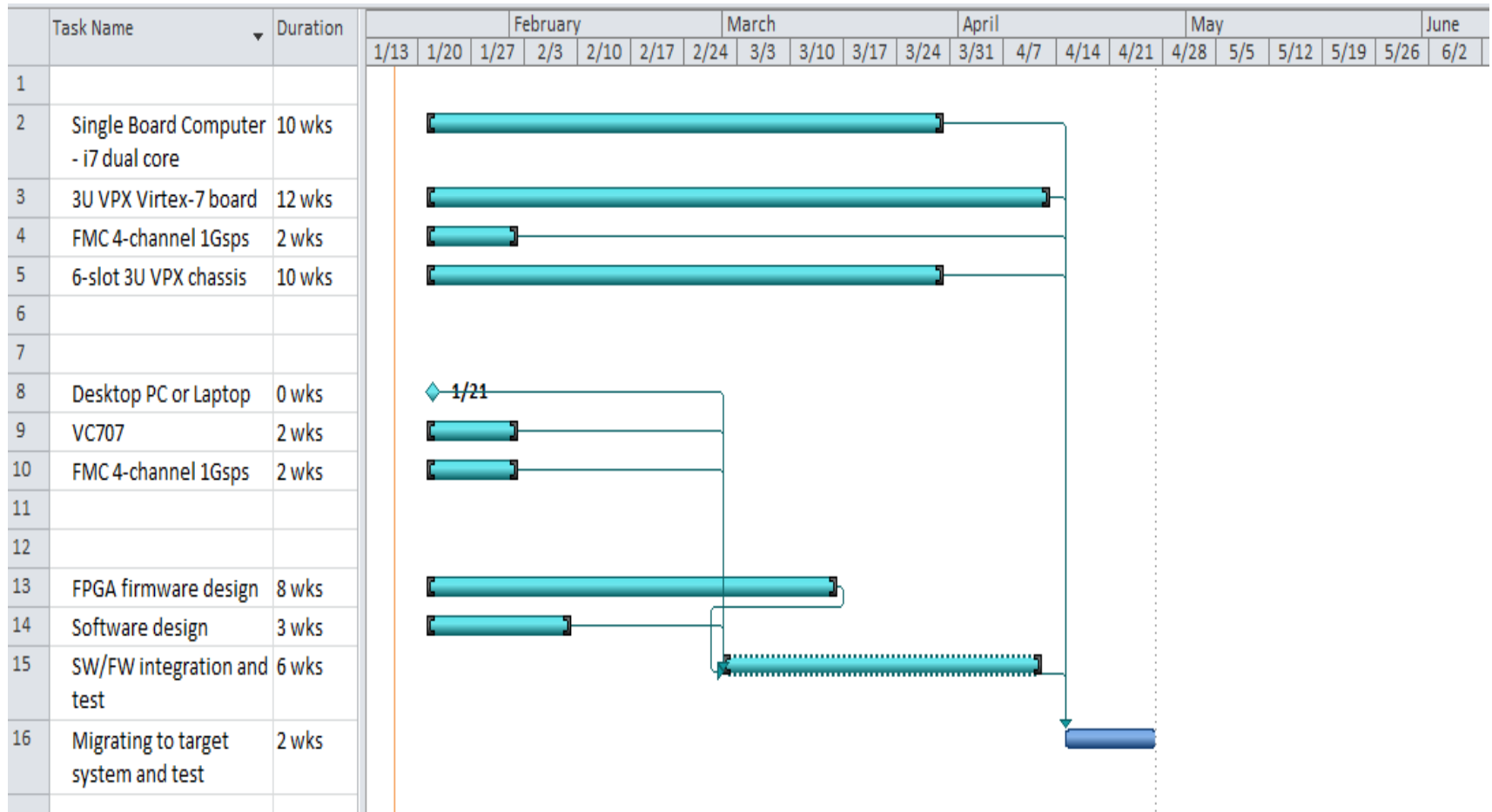
# Potential solution costs

SBC	\$5,000
FPGA Carrier	\$13,000
FMC 4 Ch 1Gbps	\$2,800
3U VPX Chassis	\$20,000
Hardware Subtotal	<b>\$40,800</b>
Firmware Design	\$23,077
Software Design	\$11,538
Engineering Labor Subtotal	<b>\$34,615</b>
Engineer overhead waiting to begin integration	<b>(\$57,692)</b>

# A complementary DAQ platform



# A risk mitigating schedule





# A program budget saving solution

VC707	\$3,500
FMC 4 Ch 1Gsps	\$2,800
<b>Dev Kit HW</b>	<b>\$6,300</b>

Engineering Overhead	\$65,385
SW/FW Int & Test Pull In	\$30,769
<b>Savings via dev kit approach</b>	<b>\$96,154</b>

# FMCs: It's becoming the standard

- FMC sites are available on most Xilinx development boards
- 70+ FMC and FMC carriers from a dozen vendors
- A/D, D/A, RF, Video, TI DSPs, touch screen, optical, etc...
- Becoming easier to integrate FMC and FMC carrier cards from different vendors (VITA 57.2)
- Reduces overall risk (shorter lead-times)
- The best I/O approach outside of a monolithic solution
- Effectively manage project budgets (cost effective solutions) for the most demanding applications

# Thank you

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<http://www.4dsp.com>

***Thank you!***